CLAIMS

We claim:

1. An apparatus executing a set of instructions, the instructions including one or more fields, wherein a field of a given instruction specifies a source of an operand of the given instruction or a destination of a result of the given instruction, and wherein the apparatus comprises:

processing means for executing the instructions; and

a register file, coupled to the processing means, for storing operands and results of the instructions, wherein,

the register file includes a plurality of register sets, and

the register file is responsive to one or more of the fields in a given instruction to retrieve an operand of the given instruction from, or store a result of the given instruction into, a given register in a given one of the register sets as identified by the one or more fields in the given instruction.

2. The apparatus of Claim 1, wherein the instructions include Boolean combinational instructions each operating on one or more Boolean operands to generate a Boolean result, each Boolean combinational instruction including one or more Boolean fields specifying a location of each operand and result, and wherein:

the processing means includes Boolean execution means for executing the Boolean combinational instructions;

the register file includes a Boolean register set of Boolean registers, each Boolean register for holding one of said Boolean operands or Boolean results; and

the register file is responsive to each said Boolean field in a given Boolean combinational instruction independent of what Boolean combinational operation is specified by the given Boolean combinational instruction.

3. The apparatus of Claim 2, wherein the instructions include Boolean comparison instructions each operating on one or more operands to generate a Boolean result, each Boolean comparison instruction including a Boolean result field specifying a location, in the Boolean register set, of the Boolean result, and wherein:

the processing means includes comparison means for executing the Boolean comparison instructions; and

the register file is responsive to the Boolean result field in a given Boolean instruction independent of what Boolean comparison operation is specified by the given Boolean comparison instruction.

4. The apparatus of Claim 1, wherein the instructions include integer instructions each operating on one or more integer operands to generate an integer result, each integer

instruction including one or more integer fields specifying a location of each operand and result, and wherein:

the processing means includes integer execution means for executing the integer instructions; and

the register file includes an integer register set of integer registers, each integer register for holding one of said integer operands or integer results.

5. The apparatus of Claim 4, wherein the register file further comprises:

a plurality of integer register sets.

6. The apparatus of Claim 1, wherein the instructions include floating point instructions each operating on one or more floating point operands to generate a floating point result, each floating point instruction including one or more floating point fields specifying a location of each operand and result, and wherein:

the processing means includes floating point execution means for executing the floating point instructions; and

the register file includes a floating point register set of floating point registers, each floating point register for holding one of said floating point operands or floating point results.

7. An apparatus comprising:

means for executing Boolean instructions, the Boolean instructions performing Boolean operations upon operands to generate Boolean results and each Boolean instruction indicating a destination for storage of the Boolean results of the Boolean instruction;

a plurality of Boolean register means each for holding a Boolean value; and

means, responsive to execution of a given Boolean instruction by said means for executing, for storing the given Boolean instruction's Boolean result into one of said Boolean register means, the one Boolean register means being indicated by said given Boolean instruction as the destination of its Boolean result.

8. The apparatus of Claim 7, wherein the means for executing Boolean instructions comprises:

numerical execution means for executing numerical comparison instructions to compare two multi-bit numerical operands and to accordingly produce a single-bit Boolean value result.

9. The apparatus of Claim 8, wherein the numerical execution means comprises:

integer execution means for comparing two multi-bit integer operands.

10. The apparatus of Claim 8, wherein the numerical execution means comprises:

floating point execution means for comparing two multi-bit floating point operands.

11. The apparatus of Claim 10, wherein the numerical execution means further comprises:

integer execution means for comparing two multi-bit integer operands.

12. The apparatus of Claim 7, wherein the means for executing Boolean instructions comprises:

Boolean execution means for executing Boolean combinational instructions to combine two Boolean value operands and to accordingly produce a single-bit Boolean value result.

13. The apparatus of Claim 12, wherein the means for executing Boolean instructions further comprises:

numerical execution means for executing numerical comparison instructions to compare two multi-bit numerical operands and to accordingly produce a single-bit Boolean value result.

14. The apparatus of Claim 13, wherein the numerical execution means comprises:

integer execution means for comparing two multi-bit integer operands; and

floating point execution means for comparing two multi-bit floating point operands.

15. The apparatus of Claim 7 further comprising:

numerical register means for holding integer and floating point values;

numerical execution means for executing numerical comparison instructions, wherein execution of each given numerical comparison instruction,

i) retrieves two or more multi-bit numerical operands from respective numerical register means specified by the given numerical comparison instruction,

ii) compares the two or more numerical operands according to a condition specified by the given numerical comparison instruction,

iii) produces a first single-bit Boolean value result according to the condition,

iv) stores the first Boolean value result in a given one of said Boolean register means as specified by the given numerical comparison instruction,

wherein the numerical execution means includes,

i) integer execution means for comparing two multi-bit integer operands, and

ii) floating point execution means for comparing two multi-bit floating point operands; and

Boolean execution means for executing Boolean combinational instructions, wherein execution of each given Boolean combinational instruction,

i) retrieves one or more Boolean value operands from respective Boolean register means as specified by the given Boolean combinational instruction,

ii) combines the one or more Boolean value operands according to an operation specified by the given Boolean combinational instruction,

iii) produces a second single-bit Boolean value result according to the operation, and

iv) stores the second Boolean value result in a given one of said Boolean register means as specified by the given Boolean combinational instruction.

16. The apparatus of Claim 7, wherein:

the plurality of Boolean register means includes,

i) a first set of Boolean registers, and

ii) a second set of Boolean registers; and the apparatus further comprises

means, coupled to the plurality of Boolean register means, for selecting the first or the second set of Boolean registers as a currently active set; and

the means for storing is responsive to the means for selecting, to store results into Boolean registers in the currently active set only.

17. An apparatus for use with a data processing system, the data processing system including means for executing Boolean instructions, each Boolean instruction performing a given Boolean operation upon two or more operands to generate a one-bit Boolean result, the apparatus comprising:

a Boolean register set including a plurality of individually addressable one-bit registers; and

control means for writing the one-bit result of a given Boolean instruction into one of said one-bit registers, the one one-bit register being specified by the given Boolean instruction's contents.

18. The apparatus of Claim 17, wherein the Boolean instructions include Boolean combinational instructions, each Boolean combinational instruction specifying a Boolean operation to be performed upon a first and a second operand to generate the result, and specifying a first address of the first operand and a second address of the second operand and a third address of a destination for the result, wherein:

the control means is further for reading the first and second operands from the Boolean register set at the first and second addresses, respectively, and wherein the one one-bit register is specified by the third address.

19. The apparatus of Claim 18, wherein the means for executing includes means for executing plural Boolean instructions in parallel, wherein there may exist, in the plural

Boolean instructions, data dependency between one or more slave instructions and a master instruction, each slave instruction having the result of the master instruction as an operand such that the slave instruction cannot be executed until the result of the master instruction has been generated, the means for executing further includes means for delaying data dependent instructions until their dependent data supplying instruction is completed and its result is generated, and wherein:

a prespecified constant Boolean register of the one-bit registers has a predetermined constant data value which does not change upon the control means writing another value to the prespecified constant Boolean register; and

the control means is responsive to a master instruction whose destination is the prespecified constant Boolean register, to immediately read the predetermined constant data value for supply to the slave instructions, whereby the means for executing is enabled to execute the slave instructions before the result of the master instruction is generated.

20. An apparatus comprising:

execution means for executing instructions, the instructions performing operations upon operands to generate results, each instruction specifying a respective source address for each operand and a destination address for the result of the instruction, each address specifying a register set and an offset;

a first register set including a plurality of individually addressable registers each for storing a value of a first data type;

first access means for writing and reading values to and from the first register set according to a given instruction, the first access means including,

i) first reading means, responsive to the given instruction having a given source address which specifies the first register set as a source for an operand of the given instruction, for reading the operand's value from the first register set at the offset specified by the given source address, and

ii) first writing means, responsive to the given instruction having a given destination address which specifies the first register set as a destination for the result of the given instruction, for writing the result's value to the first register set at the offset specified by the given destination address;

a second register set including a plurality of individually addressable registers each for storing a value of the first data type; and

second access means for writing and reading values to and from the second register set according to the given instruction, the second access means including,

i) second reading means, responsive to the given instruction having a given source address which specifies the second register set as a source for an operand of the given instruction, for reading the operand's value from the second register set at the offset specified by the given source address, and

ii) second writing means, responsive to the given instruction having a given destination address which specifies the second register set as a destination for the result of the given instruction, for writing the result's value to the second register set at the offset specified by the given destination address.

21. The apparatus of Claim 20, wherein:

a given instruction may specify a first and a second source address and a destination address, with each address specifying either of the first or second register sets such that the given instruction requires access to both register sets; and

the first and second access means operate simultaneously to provide the instruction parallel access to both the first and second register sets.

22. In a data processing system, which includes a central processing unit (CPU) which performs operations according to an instruction, the operations operating upon data of a first data type, a data register system comprising:

a first register set including a plurality of first registers each for holding a datum of the first data type, and including means for accessing the first registers in response to the instruction; and

a second register set including a plurality of second registers each for holding a datum of the first data type, and including means for accessing the second registers in response to the instruction.

23. The data register system of Claim 22, wherein the instruction includes a field specifying which of the first and second register sets is to be accessed in response to the instruction, and wherein the data register system further comprises:

means, responsive to the field, for accessing the first register set or the second register set as specified by the field.

24. An apparatus comprising:

integer execution means for executing integer instructions, each integer instruction performing an integer operation upon one or more integer value operands and generating an integer value result;

floating point execution means for executing floating point instructions, each floating point operation performing a floating point operation upon one or more floating point value operands and generating a floating point value result;

wherein each instruction specifies one or more sources from which its one or more operands are to be retrieved and further specifies a destination to which its result is to be stored, each operation also optionally specifying an integer value base and an integer value index;

a register bank including,

i) first register set means, having a plurality of first registers, for holding integer values and floating point values;

access means, coupled to the first register set means and to both execution means, for,

i) retrieving, from any one first register, an integer value operand for the integer execution means, a floating point value operand for the floating point execution means, or an integer value base or index for either execution means, as indicated by an instruction, and

ii) for storing, into any one first register, an integer value result from the integer execution means or a

floating point value result from the floating point execution means, as indicated by an instruction.

25. The apparatus of Claim 24, wherein:

the register bank further comprises second register set means, having a plurality of second registers, for holding integer values; and

the access means is further for,

i) retrieving, from any one second register, an integer value operand for the integer execution means, or an integer value base or index for either execution means, as indicated by an instruction, and

ii) for storing, into any one second register, an integer value result from the integer execution means, as indicated by an instruction.

26. The apparatus of Claim 25, further comprising:

Boolean execution means for executing Boolean combinational instructions, each Boolean combinational instruction performing a Boolean combinational operation upon one or more Boolean value operands and generating a Boolean value result;

the register bank further comprises third register set means, having a plurality of third registers, for holding Boolean values; and

the access means is further for,

i) retrieving, from any one third register, a Boolean value operand for the Boolean execution means, as indicated by a Boolean combinational instruction, and

ii) for storing, into ~~any one~~ third register, a Boolean value result from the Boolean execution means, as indicated by a Boolean combinational instruction.

27. An apparatus, for use with a data processing system which performs read operations and write operations upon data values of a first data type and a first data width and upon data values of a second data type and a second data width different than the first data width, the data processing system specifying a read address and data type for each read and a write address and data content for each write, the apparatus comprising:

a register set including a plurality of individually addressable registers, each register being wide enough to hold a value of either data width;

read access means, responsive to the data processing system performing a given read operation, for accessing the register set to retrieve data contents of a given register, which is individually addressed at the given read operation's specified read address, and for providing to the data processing system such portion of the retrieved data contents as the data type of the read operation specifies; and

write access means, responsive to the data processing system performing a given write operation, for accessing the register set to store into a given register, which is individually addressed at the given write operation's specified write address, the data content specified by the write operation.

28. The apparatus of Claim 27, wherein the first data type is floating point, the first data width is sixty-four bits, the second data type is integer, the second data width is thirty-two bits, and wherein:

the register set is sixty-four bits wide; and

the read and write access means respectively retrieve and store sixty-four bits responsive to the data processing system performing floating point operations, and thirty-two bits responsive to the data processing system performing integer operations.

29. An apparatus for use with a data processing system which executes instructions, each instruction performing operations upon one or more operands and generating a result, wherein each instruction specifies one or more sources from which its one or more operands are to be retrieved and further specifies a destination to which its result is to be stored, wherein the data processing system operates in a plurality of modes, the apparatus comprising:

a plurality of first register means each for holding an operand or a result;

a plurality of second register means each for holding an operand or a result; and

switch means, responsive to the mode of the data processing system, for providing the data processing system access to only the plurality of first register means when the data processing system operates in a first mode, and for providing the data processing system access to only a first subset of the plurality of first register means and to the plurality of second register means when the data processing system operates in a second mode.

30. An apparatus including execution means for executing instructions, each instruction performing operations on one or more operands and generating a result, each instruction specifying one or more sources which are to be accessed to read its one or more operands and a destination which is to be accessed to write its result, the apparatus further comprising:

a plurality of register banks;

each register bank including a plurality of register means, each register means for storing an operand or a result, the plurality of register means within each register bank being arranged in a sequence such that any one given register means within a given register bank may be accessed as an offset into the given register bank, wherein the sources and the destination of a given instruction are specified as offsets; and

register bank selector means for selecting a given register bank into which the given instruction's source and destination offsets are applied, the register bank selector means operating independently of any contents of the given instruction.